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Claus Schmiederer

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MICHAEL J. STRIKER
103 EAST NECK ROAD
HUNTINGTON, NY 11743

EXAMINER

THOMAS, LUCY M

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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/591,890
Filing Date: September 07, 2006
Appellant(s): SCHMIEDERER ET AL.

Michael J. Striker
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on 4/08/2010 appealing from the Office action mailed on 1/14/2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims 1-3, 5, and 7-12.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the

subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

US2003/0048029	DEDARAN	3-2003
US2003/0231451	ANTHONY	12-2003
US 5,883,335	MIZUMOTO	3-1999
FR 2,783,369	MIGNE	3-2000
US 5,229,088	HONL	3-1994

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3, 5, 7-8, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeDaran et al. (US 2003/0048029) in view of Anthony (US 2003/0231451), and Mizumoto et al. (US 5,883,335). Regarding Claim 1, DeDaran

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discloses an interference suppressor (see Figures 1, 3-5) for suppressing high-frequency interference emissions of a direct current motor 34 that is drivable in a plurality of stages and/or directions, having a plurality of capacitors 82, 84 (Figure 5) located on a first side (top side) of a printed circuit board 10 (Figure 1), 73 (Figure 4) and having a plurality of first conductor tracks 58, located on the first side of the printed circuit board, for putting the various capacitors into contact with a ground terminal 60, and having a first terminal (see terminal in Figure 5 to which one terminal of 82, and top terminal 74 of 72, and 16 are connected) and at least one second terminal (see terminal in Figure 5 to which one terminal of 84, and bottom terminal 76 of 72, and 18 are connected) for the individual stages of the direct current motor, the printed circuit board having a second side (bottom surface), diametrically opposite to the first side, and the first terminal and the at least one second terminal being put into contact with a first connection line 38 for the first stage and at least one further connection line 40 for the at least one second stage of the direct current motor.

DeDaran does not specifically disclose that a ground face is located on the second side, and the first connection line and the at least one further connection line are fed through in insulated fashion relative to the ground face, and that the ground face is electrically connected via through-plated holes or via-holes.

Anthony discloses an interference suppressor 10 (see Figures) having plurality of capacitors 30, 32 arranged on a printed circuit board with metallized ground face 14 (Figure 1), 112 (Figures 2-5, 9) and with insulating apertures 18 (Figure 1), 114 (Figures 2-5, 9) for connection lines 12, 118 to be fed through in an insulative fashion to the

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ground face (see Paragraphs 24, 76, 93). Anthony also teaches that the capacitor electrode bands 2028 of the capacitive filter 2012 are connected to the connectors 2024 through-hole plating 2020 and conductive pads embodied as via holes with conductive epoxy filling the hole, and one of the connector is connected to ground terminal (see for example Figures 9D, 12, Paragraphs 106, 107, 109). Anthony does not specifically disclose the connection between the ground surface and the terminal.

Mizumoto discloses an electrical connection structure (Figures 1-9, Abstract) for electrically connecting a chip 10 (Figures 2-3) on of a printed circuit board 200, 300 (Figures 2-3), the printed circuit board having a first/mounting surface 332 and second/back surface 334 (Abstract, Column 4, lines 56-3, Claims) with power supply, signal and ground lines built on the substrate 290 of the printed circuit board (Column 5, lines 50-54), and having a through-hole 5 or 50 (Figure 5) and via hole 3 (Figure 1) 28, 29 (Figures 4, 7-9) to connect the lines of the mounting surface with that of the back surface (Column 5, lines 54-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the surge suppressor of DeDaran with a ground face on the diametrically opposite surface, and connect the ground face to the ground terminals with via holes, because Anthony teaches the use of through-plated holes embodied as via holes and metallized ground surface to provide a significantly large ground plane which helps with attenuation of radiated electromagnetic emissions and provides a greater surface area in which to dissipate over voltages and surges (see Anthony, Paragraph 75), and Mizumoto teaches through-hole and via hole for connecting lines of

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a chip on the mounting surface, to the connecting terminals/lines on the opposite surface and that via holes can be used to increase degree of freedom of the wiring between the two surfaces and/or between layers of the PCB and to shorten wiring length from the chip to the connecting terminal/solder bump on the opposite surface (see Mizumoto, Column 1, lines 52-61, Column 4, lines 1-3).

Regarding Claim 2, DeDaran discloses that at least one peak limiting devices/varistor and/or at least one capacitor 72 is located on the first side of the printed circuit board and is connected to the first terminal and the at least one further terminal, respectively, via second conductor tracks (see Paragraph 71).

Regarding Claim 3, DeDaran discloses that that the conductor tracks are located on the first side of the printed circuit board symmetrically about an axis of the printed circuit board (see Figures 1, 4). Regarding Claim 6, Anthony discloses that the through-plated holes are embodied as via-holes (thru-hole plating 2020 of apertures 2018 recited in Paragraph 109).

Regarding Claim 5, DeDaran discloses that the capacitors are embodied as SMD ceramic capacitors (Paragraph 57).

Regarding Claims 7-8, Anthony discloses a shielding housing (see enclosure or grounded chassis recited in Paragraph 76), surrounding the interference suppressor, which housing is connected electrically conductively to the ground face, and that the first connection line and the at least one second connection line are fed through the shielding housing (see Figure 1A).

Regarding Claim 12, DeDaran discloses that the capacitors and/or the at least one varistor and/or the at least one capacitor is contacted by way of radial or axial connection wires extended to the outside.

3. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeDaran et al. (US 2003/0048029) in view of Anthony (US 2003/0231451), Mizumoto et al. (US 5,883,335) and Migne (FR 2 783 369). Regarding Claim 9-10, DeDaran and Anthony do not specifically disclose that the shielding housing is connected electrically conductively to a motor housing of the direct current motor, via a plurality of contact points. Migne discloses a surge suppressor circuit on a printed circuit board for a DC motor, which is electrically conductively connected to a motor housing of the DC motor (see Abstract, Figures 1-4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of DeDaran, Mizumoto, and Anthony, and to have the shielding housing/carrier connection in a motor housing to reduce noise and spikes, because Migne teaches the use of such a connection in a DC motor.

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over DeDaran et al. (US 2003/0048029) in view of Anthony (US 2003/0231451), Mizumoto et al. (US 5,883,335), and Honl et al. (US 5,299,088). Regarding Claim 11, DeDaran and Anthony do not disclose that at defined points, the conductor tracks have tapered portions for a short-circuit guard. Honl discloses a protective circuit wherein conductor tracks 63, 65 have tapered portions 70, 71 for short circuit protection (see Figure 7, Column 7, lines 45-50). It would have been obvious to one of ordinary skill in the art at

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the time the invention was made to modify the combination of DeDaran, Mizumoto, and Anthony, and to provide tapered or narrow portions on the conductive tracks for short circuit protection as taught by Honl, because tapered portions in the conductive tracks provide short circuit protection by forming fuse regions between the tracks and ground (see Honl, Column 7, lines 45-50).

(10) Response to Argument

Appellant's arguments regarding the obviousness rejection of Claims 1, 5, 7-8 and 12 over DeDaran et al. (US 2003/0048029) in view of the Anthony et al. (US 2003/0231451) and Mizumoto et al. (US 5,883,335).

The Appellant argues, on Page 9 of the Appeal Brief that the secondary reference Anthony does not have a ground face electrically connected via through-plated holes embodied as via-holes to ground terminals of capacitors on a first side of printed circuit board, wherein the via-holes are electrically conductive sleeves which are filled with a highly conductive metal.

Examiner respectfully disagrees. As shown above in the rejection of Claim 1, Anthony discloses an interference suppressor 10 (see Figures) having plurality of capacitors 30, 32 arranged on a printed circuit board with metallized ground face 14 (Figure 1), 112 (Figures 2-5, 9) and with insulating apertures 18 (Figure 1), 114 (Figures 2-5, 9) for connection lines 12, 118 to be fed through in an insulative fashion to the ground face (see Paragraphs 24, 76, 93). In Figure 12 Anthony teaches that the capacitor electrode bands 2028 of the capacitive filter 2012 are connected to the connectors 2024 through-hole plating 2020 and conductive pads embodied as via holes

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with conductive epoxy filling the hole, and one of the connector is connected to ground terminal (see also Paragraphs 106, 107, 109).

In paragraph 107, Anthony discloses, "through-hole plating 2020 provides greater surface area for electrical coupling of conductors 2034 to conductive pads 2024 as the conductors 2034 are disposed through apertures 2018. The configuration of the metalized ground surface 2016, insulating bands 2022 and conductive pads 2024 provide the necessary contacts for connecting a surface mount component, such as differential and common mode filter 2012, to the upper surface of carrier 2010, which in turn provides electrical connection between conductors 2034 and surface mount component 2012." Regarding the embodiment of Figure 3, in Paragraph 84, Anthony discloses, "Although not shown, electrical conductors pass through the common ground conductive plates 112 and the respective conductive electrodes. Connections are either made or not made through the selection of coupling apertures 120 and insulating apertures 114." As acknowledged in the office action, in Figure 12 which shows the through-hole and metalized ground surface, Anthony does not specifically disclose the connection between the ground surface 2016 and the terminal.

Examiner further notes that in Paragraph 93, Anthony references teaches "various conductive electrodes and common conductive plates, chassis and board noise blocking capacitors are formed by the interaction of common ground conductive plates 112 and blocking electrodes 682 and 684. For instance, chassis is connected to the electrical conductors 1 and 7, both of which are electrically connected through coupling apertures 120.." See also Paragraphs 24, 76, 109 of Anthony. The thru-hole plating

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2020 allows conductors 2034 and conductive pads 2024 adhering to the thru-hole plating, and at least one of the conductors or conductive electrodes 2034 has connection to ground surface to dissipates interferences or over voltages (see also reciting of Paragraph 93 above).

The Appellant argues, on Pages 9-10 of the Appeal Brief that Mizumoto reference also does not have a ground face electrically connected via through-plated holes embodied as via-holes to ground terminals of capacitors on a first side of printed circuit board, wherein the via-holes are electrically conductive sleeves which are filled with a highly conductive metal.

In response, examiner notes that the Anthony reference is relied upon for the teaching of ground surface 2016 as shown in the rejection and discussed above. Anthony does not specifically disclose the connection between the ground surface 2016 and the terminal. Mizumoto reference is relied upon for the connection between the terminals of chip on the mounting surface of a PCB and the terminals on the opposite surface of the PCB through through-holes and via holes.

The Appellant argues, on Pages 10-11 of the Appeal Brief that Anthony and Mizumoto references do not contain any hint, suggestion or motivation for modifying the primary reference DeDaran.

Examiner respectfully disagrees. In Paragraph 65, Anthony teaches the need for interference free connection in various applications, and in Paragraph 69, teaches the need to provide a low impedance connection, "to reduce, minimize, or suppress noise it is necessary to provide a low impedance path to ground while simultaneously

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shortening the overall noise current loop.” It is also noted that the device of the instant application (see Claim 5) is built as surface mount device.

Anthony discloses in Paragraph 107, the motivation to use through-plated holes, “through-hole plating 2020 provides greater surface area for electrical coupling of conductors 2034 to conductive pads 2024 as the conductors 2034 are disposed through apertures 2018.”

Mizumoto teaches the use of through-holes and via-holes for connecting terminals/lines on a mounting surface to those on an opposite surface and that via holes can be used to increase degree of freedom of the wiring between the two surfaces and/or between layers of the PCB and to shorten wiring length from the chip to the connecting terminal/solder bump on the opposite surface (see Mizumoto, Column 1, lines 52-61, Column 4, lines 1-3).

Regarding Appellant’s arguments toward the obviousness rejection of Claims 9-10 and 11 over DeDaran et al. (US 2003/0048029) in view of the Anthony et al. (US 2003/0231451), Mizumoto et al. (US 5,883,335), and Migne (FR 2, 783, 369) and Claim 11 over DeDaran et al. (US 2003/0048029) in view of the Anthony et al. (US 2003/0231451), Mizumoto et al. (US 5,883,335), and Honl et al. (US 5, 299, 088), please see the response to arguments toward Claim 11 above.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner’s answer.

For the above reasons, it is believed that the rejections should be sustained.

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Respectfully submitted,

/Lucy Thomas/

Examiner, Art Unit 2836

/Jared J. Fureman/

Supervisory Patent Examiner, Art Unit 2836

Conferees:

/Jared J. Fureman/

Supervisory Patent Examiner, Art Unit 2836

/Justin P. Bettendorf/

RQAS, TC 2800